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| EXAMINER | |
|---|---|
| STEVENS, THOMAS H | |
| **ART UNIT** | **PAPER NUMBER** |
| 2123 | |

DATE MAILED: 06/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| *Office Action Summary* | **Application No.** | **Applicant(s)** | |
|---|---|---|---|
| | 09/832,933 | WU ET AL. | |
| | **Examiner** | **Art Unit** | |
| | Thomas H. Stevens | 2123 | |

***-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --***

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *06 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-7,9-20,22-39,52-58,61-65,76,77 and 91-104* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-20,22-39,52-58,61-65,76,77 and 91-104* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

WILLIAM THOMSON
SUPERVISORY PATENT EXAMINER

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 1/12/02
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-7,9-20, 22-39,52-58,61-65,76,77 and 91-98 were previously examined.

2. Claims 99-104 were added.

3. Claims 1-7,9-20, 22-39,52-58,61-65,76,77 and 91-104 were examined.

### *Section I: Non-Final Rejection (2nd Office Action)*

Information Disclosure Statement

4. The information disclosure statement filed 9/12/02 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered. In this instance, the Leblebici et al. reference is missing.

### *Claim Objections*

5. Claim 76, line 10 has a typographical error: "derived form".

6. Claim 91 is objected to since the dependent apparatus claim is linked to an independent method claim.

### *Claim Objections based on Antecedent Basis Issues*

7. The examiner has provided a number of examples of objected dependent claim deficiencies based on antecedent rejected claims; however, the list of deficiencies may not be all-inclusive. Applicants should referrer to these as examples of deficiencies and initiate all necessary amendments to eliminate claim objections:

- Claim 1 recites the limitation "the behavior " in line 6.
- Claims 20 and 36 recites the limitation "the same function " in line 2.
- Claim 61 recites the limitation "the time dependence" and "the drain current" in line 3.
- Claim 55 is objected to by the limitations of " the current magnitude", "the respective current" and "the current magnitude".
- Claims 61-63, and 65 are objected to the limitation of "the aging".
- Claims 62 and 63 are objected to by the "time dependence" limitation.
- Claim 97 recites the limitation "the aging" in line 2.

### *Claim Rejections - 35 USC § 112*

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 1-7,9-20, 22-39,52-58,61-65,76,77, 92-104 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

10. Claim 1 recites the limitation "the degradation" in line 1. There is insufficient antecedent basis for this limitation in the claim.

11. Claim 1 recites the limitation "the components" in line 3. There is insufficient antecedent basis for this limitation in the claim.

12. Claim 1 recites the limitation "the fresh circuit" in line 6. There is insufficient antecedent basis for this limitation in the claim.

13. Claim 1 recites the limitation "the operation" in lines 8 and 9. There is insufficient antecedent basis for this limitation in the claim.

14. Claims 18 and 19 recites the limitation "the same device type" in line 2. There is insufficient antecedent basis for this limitation in the claims.

15. Claims 34 and 35 recites the limitation "the same device type" in line 2. There is insufficient antecedent basis for this limitation in the claims.

16. Claim 54 recites the limitation "the source" in line 3. There is insufficient antecedent basis for this limitation in the claim.

17. Claim 55 recites the limitation " the respective current" in lines 2. There is insufficient antecedent basis for this limitation in the claim.

18. Claim 55 recites the limitation" the values" and " the coefficients" in line 5. There is insufficient antecedent basis for this limitation in the claim.

19. Claim 62 recites the limitation "the substrate current" in line 2. There is insufficient antecedent basis for this limitation in the claim.

20. Claim 63 recites the limitation "the gate current" in line 2. There is insufficient antecedent basis for this limitation in the claim.

21. Claim 64 recites the limitation "the intermediate circuit stress time value" in lines 10-13. There is insufficient antecedent basis for this limitation in the claim.

22. Claim 76 recites the limitation "the non-aged version" in line 6. There is insufficient antecedent basis for this limitation in the claim.

23. Claim 76 recites the limitation "the revised netlist " in line 10. There is insufficient antecedent basis for this limitation in the claim.

24. Claim 92 recites the limitation " the behavior" and "the fresh circuit" in line 10. There is insufficient antecedent basis for this limitation in the claim.

25. Claim 92 recites the limitation "the degraded operation" in line 13. There is insufficient antecedent basis for this limitation in the claim.

26. Claim 92 recites the limitation " the operation" in line 14. There is insufficient antecedent basis for this limitation in the claim.

27. Claims 95 recite the limitation "the magnitude" in lines 2 and 5, respectively. There is insufficient antecedent basis for this limitation in the claim.

28. Claim 95 recites the limitation " the current magnitude" in line 5. There is insufficient antecedent basis for this limitation in the claim.

29. Claim 100 recites the limitation "the degradation level" in line 6 and "the respective specified degradation level" in lines 12 and 13. There is insufficient antecedent basis for this limitation in the claim.

30. Claim 101 recites the limitation "the terminals" in line 4. There is insufficient antecedent basis for this limitation in the claim.

Due to the number of 35 USC § 112-second paragraph rejections, the examiner has provided a number of examples of the claim deficiencies in the above rejections; however, the list of rejections may not be all-inclusive. Applicant should refer to these rejections as examples of deficiencies and should initiate all corrections to abrogate 35 USC § 112-second issues and place the claims in a proper format.

Due to the vagueness and lack of clear definition of the terminology and phrases used in the specification and claims, the claims have been treated on their merits as best understood by the examiner.

### *Claim Rejections - 35 USC § 103*

31. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

32. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

33. Claims 1-7,9-20, 22-39,52-58,61-65,76,77, 91,92-104 are rejected under 35 U.S.C. 103 (a) as being unpatented over Kadoch et al. (US Patent 5,761,481) (hereafter Kadoch), in view of Rajgopal et al. (hereafter Rajgopal) and in further view of Chen et al. titled "A Unified Compact Scalable Model for Hot Carrier Reliability Simulation" (hereafter Chen). All three references are analogous art because they all teach circuit simulation/modeling.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the functional blocks of Rajgopal and the circuit degradation simulation of Chen in the of the single run simulation of Kadoch because Rajgopal teaches a need for such a power estimation tool which makes it easier for the designer to determine the power usage of the system (Rajgopal: column 2, lines 2-4). Chen teaches excellent accuracy under all regions for a full range of stress conditions and excellent scalability (Chen: pg. 247, Summary, lines 7-9).

Claim 1. A method of simulating (Chen: introduction, 2nd paragraph, line 7) the degradation of a circuit (Chen: "MOSFET degradation", introduction, 1st sentence), comprising: providing a netlist (Rajgopal: column 5, line 63) specifying the components (Rajgopal: column 8, lines 40-42) of the circuit; supplying a plurality of circuit stress time (Chen: pg. 246, figure 5, plurality of stress times) values (Chen: pg. 246, figure 5, a plurality of different stress times); supplying aging model (Chen: pg. 244 "Model Formation" equation 1 "Age parameter") information on selected ones of the components; simulating the behavior (Chen: pg.245, right column, lines 13 and 14) of the fresh circuit (Chen: pg.243, left column, 2nd paragraph, lines 9-10)to determine for each of the selected components (Rajgopal: column 8, lines 40-42) a component degradation parameter (Chen: pg. 243, left column 2nd paragraph, line 6)relative to circuit stress time (Chen: pg. 246, figure 5, plurality of stress times); and determining the degradation parameter (Chen: pg. 243, left column 2nd paragraph, line 6) relative to circuit by simulating the in a single run (Kadoch: column 2, line 62) operation of the circuit with the specified components (Rajgopal: column 8, lines 40-42) using their respective aging model (Chen: pg. 244 "Model Formation" equation 1 "Age parameter") information and respective relative component degradation parameter at the plurality supplied circuit stress time (Chen: pg. 246, figure 5, plurality of stress times) values.

Claim 2. The method of claim 1, wherein said degradation of the circuit is due to hot-carrier effects (Chen: title).

Claim 3. The method of claim 1, wherein the simulating is performed using a SPICE (Chen: Introduction, left column, 2nd paragraph) type circuit simulator.

Claim 4. The method of claim 1, wherein the simulating is performed using a timing simulation (Chen: pg.246, figure 5, "stress time") type circuit simulator.

Claim 5. The method of claim 1, wherein the aging model (Chen: pg. 244 "Model Formation" equation 1 "Age parameter") information on the selected ones of the components (Rajgopal: column 8, lines 40-42) is derived from electrical test data.

Claim 6. The method of claim 1, wherein said simulating the behavior (Chen: pg.245, right column, lines 13 and 14) of the fresh circuit (Chen: pg.243, left column, 2nd paragraph, lines 9-10) determines the waveforms at the nodes (Chen: pg.247, figure 10 response from fresh circuit model) to which the selected ones of the components (Rajgopal: column 8, lines 40-42) are connected relative to an input waveforms.

Claim 7. The method of claim 1, wherein determining the degraded operation of the circuit comprises determining the circuit's speed at the supplied circuit age (Chen: pg. 244, equation 2 with right column, lines 4-8) parameters.

Claim 9. The method of claim 93, wherein the distinct sets of components (Rajgopal: column 8, lines 40-42) each form different functional blocks (Rajgopal: column 7, line 21).

Claim 10. The method of claim 8, wherein a first of said sets of components (Rajgopal: column 8, lines 40-42) is an analog block and a second of said sets of components (Rajgopal: column 8, lines 40-42) is a digital block.

Claim 11. The method of claim 10, wherein the performance criterion of the first set is transconductance (Kadoch: column 1, line 34) and the performance criterion of the second set is drain (Chen: pg.244, line 5) to source current.

Claim 12. The method of claim 8, wherein the distinct sets of components (Rajgopal: column 8, lines 40-42) consist of different device types (resistors, capacitors, transistors, etc.).

Claim 13. The method of claim 12, wherein a first of said different device types is an NMOS and a second of said different device types is a PMOS (MOSFETS cover NMOS and PMOS, well-known).

Claim 14. The method of claim 13, wherein the PMOS (MOSFETS cover NMOS and PMOS, well-known) performance criterion is leakage current (Kadoch: column 1, line 34).

Claim 15. The method of claim 13, wherein the NMOS performance criterion is driving capability (Chen: pg.243, right column, 3rd paragraph, "forward/reverse operation" of degradation device)).

Claim 16. The method of claim 12, wherein a first of said different device types is a MOSFET (Chen: pg. 243, Introduction, left column, 1st paragraph) and a second of said different device types is a bipolar junction Transistor (i.e., JFETs well-known).

Claim 17. The method of claim 16, wherein the bipolar junction transistor performance criterion is leakage current (Kadoch: column 1, line 34).

Claim 18. The method of claim 93, wherein the distinct sets of components (Rajgopal: column 8, lines 40-42) employ different models for simulating the same device type.

Claim 19. The method of claim 93, wherein the distinct sets of components (Rajgopal: column 8, lines 40-42) consist of the same device type.

Claim 20.The method of claim 93, wherein the distinct sets of components (Rajgopal: column 8, lines 40-42) form functional blocks (Rajgopal: abstract, line 8) performing the same function.

Claim 22. The method of claim 94, wherein the first and second sets of components (Rajgopal: column 8, lines 40-42) each form different functional blocks (Rajgopal: column 7, line 21) (Rajgopal: abstract, line 8).

Claim 23. The method of claim 94, wherein the second set components (Rajgopal: column 8, lines 40-42) form a digital block.

Claim 24. The method of claim 23, wherein the specified degradation level is expressed in terms of drain (Chen: pg.244, line 5).

Claim 25. The method of claim 94, wherein the second set of components (Rajgopal: column 8, lines 40-42) is an analog block.

Claim 26. The method of claim 25, wherein the specified degradation level is expressed in terms transconductance (Kadoch: column 1, line 34) degradation.

Claim 27. The method of claim 94, wherein the first and second sets of components (Rajgopal: column 8, lines 40-42) each consist of different device types (transistors, capacitors, etc.).

Claim 28. The method of claim 27, wherein the second set of components (Rajgopal: column 8, lines 40-42) consists of PMOS transistors (well-known).

Claim 29. The method of claim 28, wherein the specified degradation level is expressed in terms of leakage current (Kadoch: column 1, line 34) degradation (Chen: pg. 243, Introduction, left column, 2nd paragraph, line 6).

Claim 30. The method of claim 27, wherein the second set of components (Rajgopal: column 8, lines 40-42) consists of NMOS transistors (well-known).

Claim 31. The method of claim 30, wherein the specified degradation level is expressed in terms of driving capability (Chen: pg.243, right column, 3rd paragraph, "forward/reverse operation" of degradation device)) degradation.

Claim 32. The method of claim 27, wherein the second set of components (Rajgopal: column 8, lines 40-42) consists of bipolar junction transistors (well-known).

Claim 33. The method of claim 32, wherein the specified degradation level is expressed in terms of leakages current (Kadoch: column 1, line 34) degradation (Chen: pg. 243, Introduction, left column, 2nd paragraph, line 6).

Claim 34. The method of claim 94, wherein the first and second sets of components (Rajgopal: column 8, lines 40-42) employ different models for simulating the same device type.

Claim 35. The method of claim 94, wherein the first and second sets of components (Rajgopal: column 8, lines 40-42) each consist of the same device type.

Claim 36. The method of claim 94, wherein the first and second sets of components (Rajgopal: column 8, lines 40-42) form functional blocks (Rajgopal: abstract, line 8) performing the same function.

Claim 37. The method of claim 94, wherein the degradation level of the second set of selected components (Rajgopal: column 8, lines 40-42) is specified as a relative component degradation parameter (Chen: pg. 243, left column 2nd paragraph, line 6)with respect to the component degradation parameter (Chen: pg. 243, left column 2nd paragraph, line 6) of the first set of components.

Claim 38. The method of claim 94, wherein the degradation level of the second set of selected components (Rajgopal: column 8, lines 40-42)is expressed in terms of age (Chen: pg. 244, equation 2).

Claim 39. The method of claim 94, wherein the degradation level of the second set of selected components (Rajgopal: column 8, lines 40-42) is expressed in terms of lifetime (Chen: pg.244, line 7).

Claim 52. The method of claim 95, wherein the selected components (Rajgopal: column 8, lines 40-42) are MOSFETs (pg. 301, left column, 3rd paragraph).

Claim 53. The method of claim 95, wherein said degradation of the circuit is due to hot carrier effects (Chen: title).

Claim 54. The method of claim 52, wherein for each of said selected components (Rajgopal: column 8, lines 40-42) more than one of said plurality of independent current sources are connected between the source and drain (Chen: pg.244, line 5) terminals of the non-aged ("Fresh" Chen, pg. 247, figure 11) version.

Claim 55. The method of claim 52, wherein said method further includes: determining the magnitude of the respective current in each of the independent current sources, (Chen: pg. 246, figure 5) said determining comprising: supplying a physical model of the

current magnitude (Chen: pg. 246, figure 5); and establishing the values of the coefficients (Chen: pg. 246, equation 7, coefficients "A, B, C") in the physical model from electrical test data.

Claim 56. The method of claim 52, wherein the degradation level of the selected components (Rajgopal: column 8, lines 40-42) is expressed in terms of lifetime (Chen: pg.244, line 7).

Claim 57. The method of claim 52, wherein the degradation level of the selected components (Rajgopal: column 8, lines 40-42) is expressed in terms of age.

Clam 58. The method of claim 95, wherein said simulating the operation of the circuit is performed with a circuit simulator and wherein said revising the netlist (Rajgopal: column 5, line 63) is embedded in the circuit simulator.

Claim 61. The method of claim 97, wherein the selected components (Rajgopal: column 8, lines 40-42)are MOSFETs and said incorporating the aging of the selected components (Rajgopal: column 8, lines 40-42) comprises including the time dependence of the drain (Chen: pg.244, line 5) to source current.

Claim 62. The method of claim 61, wherein said incorporating the aging of the selected components (Rajgopal: column 8, lines 40-42) comprises including the time dependence of the substrate current.

Claim 63. The method of claim 61, wherein said incorporating the aging of the selected components (Rajgopal: column 8, lines 40-42) comprises including the time dependence of the gate current (Chen: pg. 244, right column "Gate Bias Dependency").

Claim 64. The method of claim 97, wherein said simulating the behavior (Chen: pg.245, right column, lines 13 and 14) of the circuit to determine for each of the selected components (Rajgopal: column 8, lines 40-42)a component degradation parameter (Chen: pg. 243, left column 2nd paragraph, line 6) relative to circuit age (Chen: pg. 244, equation 2 with right column, lines 4-8) comprises: simulating the behavior (Chen: pg.245, right column, lines 13 and 14) of the fresh circuit (Chen: pg.243, left column, 2nd paragraph, lines 9-10 )to determine for each of the selected components (Rajgopal: column 8, lines 40-42)an intermediate component degradation parameter (Chen: pg. 243, left column 2nd paragraph, line 6) relative to circuit stress time (Chen: pg. 246, figure 5, plurality of stress times); determining the degraded operation of the circuit at an intermediate circuit stress time (Chen: pg. 246, figure 5, plurality of stress times) value by simulating the operation of the circuit with each of the specified components (Rajgopal: column 8, lines 40-42) using the respective aging model (Chen: pg. 244 "Model Formation" equation 1 "Age parameter") information and respective relative

intermediate component degradation parameter (Chen: pg. 243, left column 2nd paragraph, line 6)at the intermediate circuit stress time (Chen: pg. 246, figure 5, plurality of stress times) value; and simulating the behavior (Chen: pg.245, right column, lines 13 and 14) of the degraded circuit at the intermediate circuit stress time (Chen: pg. 246, figure 5, plurality of stress times) value to determine for each of the selected components (Rajgopal: column 8, lines 40-42) a component degradation parameter (Chen: pg. 243, left column 2nd paragraph, line 6) relative to circuit age, (Chen: pg. 244, equation 2 with right column, lines 4-8) wherein the intermediate circuit stress time (Chen: pg. 246, figure 5, plurality of stress times) value is less than one of the circuit stress time (Chen: pg. 246, figure 5, plurality of stress times) values (Chen: pg. 246, figure 5, a plurality of different stress times).

Claim 65. The method of claim 97, wherein said simulating the operation of the circuit is performed with a circuit simulator and wherein said incorporating the aging of the selected components (Rajgopal: column 8, lines 40-42) by updating the modules of said circuit simulator is embedded in the circuit simulator.

Claim 76. The method of claim 98, wherein said determining comprises: revising the netlist (Rajgopal: column 5, line 63), wherein each of said selected components (Rajgopal: column 8, lines 40-42) is replaced by a non-aged ("Fresh" Chen, pg. 247, figure 11) version of the selected component and a plurality of independent current sources corresponding to different mechanisms with distinct quantized (age times as

stated in spec. pg.6, lines 19-26: Chen pg. 246, figure 5 plurality of stress times or age times) relative degradation level connected between the terminals of the non-aged ("Fresh" Chen, pg. 247, figure 11) version, the magnitude of the respective quantized (age times as stated in spec. pg.6, lines 19-26: Chen pg. 246, figure 5 plurality of stress times or age times) current in each of the current sources determined from the aging model (Chen: pg. 244 "Model Formation" equation 1 "Age parameter") information of component; and determining the degraded operation of the circuit by simulating the operation of the circuit with the revised netlist (Rajgopal: column 5, line 63), the independent current magnitudes derived form the respective aging model (Chen: pg. 244 "Model Formation" equation 1 "Age parameter") information and respective relative degradation level at the supplied circuit stress time (Chen: pg. 246, figure 5, plurality of stress times) value.

Claim 77. The method of claim 98, wherein said simulating the operation of the circuit is performed with a circuit simulator and wherein said quantizing (age times as stated in spec. pg.6, lines 19-26: Chen pg. 246, figure 5 plurality of stress times or age times) is embedded in the circuit simulator (Chen: Introduction, left column, 2nd paragraph, "SPICE").

Claim 91. A computer readable storage device embodying a program of instructions executable by a computer (Chen: Introduction, left column, 2nd paragraph, "SPICE" computer software model) to perform the method of any one of claims 1 and 93-98.

Claim 92. A method for transmitting a program of instructions executable by a computer to perform a process of simulating the degradation of a circuit (Chen: "MOSFET degradation", introduction, 1st sentence), said method comprising: causing the transmission to a client (Kadoch: column 2, line 6) device a program of instructions, thereby enabling the client device to perform, by means of such program, the process simulating the degradation of a circuit (Chen: "MOSFET degradation", introduction, 1st sentence), comprising: providing a netlist (Rajgopal: column 5, line 63) specifying the components (Rajgopal: column 8, lines 40-42) of the circuit; supplying a plurality of circuit stress time (Chen: pg. 246, figure 5, plurality of stress times) values (Chen: pg. 246, figure 5, a plurality of different stress times); supplying aging model (Chen: pg. 244 "Model Formation" equation 1 "Age parameter") information on selected ones of the components; simulating the behavior (Chen: pg.245, right column, lines 13 and 14) of the fresh circuit (Chen: pg.243, left column, 2nd paragraph, lines 9-10)to determine for each of the selected components (Rajgopal: column 8, lines 40-42) a component degradation parameter (Chen: pg. 243, left column 2nd paragraph, line 6) relative to circuit stress time (Chen: pg. 246, figure 5, plurality of stress times); and determining the degraded operation (Chen: pg. 247, figure 11, comparisons between "Fresh", and "Aged Model") of the circuit by simulating in a single run (Kadoch: column 2, line 62) the operation of the circuit with the specified components (Rajgopal: column 8, lines 40-42) using their respective aging model (Chen: pg. 244 "Model Formation" equation 1 "Age parameter") information and respective relative component degradation parameter

(Chen: pg. 243, left column 2nd paragraph, line 6) at the plurality of supplied circuit stress time (Chen: pg. 246, figure 5, plurality of stress times) values (Chen: pg. 246, figure 5, a plurality of different stress times).

Claim 93. The method of claim 1, wherein the circuit includes a plurality of distinct sets of components (resistors, capacitors, transistors, etc.), the method further comprising: supplying an independent performance criterion for each set of said plurality of distinct sets of components (Rajgopal: column 8, lines 40-42) from each of said sets of components, wherein each of the selected components' relative degradation parameter (Chen: pg. 243, left column 2nd paragraph, line 6) is determined using the respective performance criteria (Rajgopal: column 2, lines 5-6) of the set to which the selected component belongs, and wherein said determining the degraded operation of the circuit includes determining the degraded operation of the circuit by simulating the operation of the circuit with each of the specified components (Rajgopal: column 8, lines 40-42)using eh respective aging model (Chen: pg. 244 "Model Formation" equation 1 "Age parameter") information and respective relative component degradation parameter (Chen: pg. 243, left column 2nd paragraph, line 6) at the supplied circuit stress time (Chen: pg. 246, figure 5, plurality of stress times) values (Chen: pg. 246, figure 5, a plurality of different stress times).

Claim 94. The method of claim 1, wherein said supplying aging model (Chen: pg. 244 "Model Formation" equation 1 "Age parameter") information includes supplying aging

model (Chen: pg. 244 "Model Formation" equation 1 "Age parameter") information on a first set of selected components (Rajgopal: column 8, lines 40-42) of the circuit and wherein said simulating the behavior (Chen: pg.245, right column, lines 13 and 14) of the fresh circuit (Chen: pg.243, left column, 2nd paragraph, lines 9-10) includes simulating the behavior (Chen: pg.245, right column, lines 13 and 14) of the fresh circuit (Chen: pg.243, left column, 2nd paragraph, lines 9-10)to determine for each of the first selected set of components (Rajgopal: column 8, lines 40-42)a component degradation parameter (Chen: pg. 243, left column 2nd paragraph, line 6) relative to circuit stress time (Chen: pg. 246, figure 5, plurality of stress times), the method further comprising: specifying the degradation level of a second set of selected components (Rajgopal: column 8, lines 40-42)of the circuit, wherein the elements of the first set and the second set of components (Rajgopal: column 8, lines 40-42) are distinct, and wherein said determining the degraded operation of the circuit includes determining the degraded operation of the circuit by simulating the operation of the circuit by simulating the operation of the circuit with each of the first set of specified components (Rajgopal: column 8, lines 40-42) using the respective aging model (Chen: pg. 244 "Model Formation" equation 1 "Age parameter") information and respective relative component degradation parameter (Chen: pg. 243, left column 2nd paragraph, line 6)at the supplied circuit stress time (Chen: pg. 246, figure 5, plurality of stress times) values (Chen: pg. 246, figure 5, a plurality of different stress times) and with each of the second set of specified components (Rajgopal: column 8, lines 40-42)using the respective specified degradation level.

Claim 95. The method of claim 1, further comprising: revising the netlist (Rajgopal: column 5, line 63), wherein each of said selected components (Rajgopal: column 8, lines 40-42) is replaced by a non-aged version of the selected components (Rajgopal: column 8, lines 40-42) and a plurality of independent current sources corresponding to different mechanisms connected between the terminals of the non-aged ("Fresh" Chen, pg. 247, figure 11) version, wherein the magnitude of the current relative to a circuit stress time (Chen: pg. 246, figure 5, plurality of stress times) in each of the current sources of a component is determined from the aging model (Chen: pg. 244 "Model Formation" equation 1 "Age parameter") information of the component and a distinct mechanism degradation parameter (Chen: pg. 243, left column 2nd paragraph, line 6) derived from the component degradation parameter; and wherein said determining the degraded operation of the circuit includes determining the degraded operation of the circuit by simulating the operation of the circuit with the revised netlist (Rajgopal: column 5, line 63) at the supplied circuit stress time (Chen: pg. 246, figure 5, plurality of stress times) values (Chen: pg. 246, figure 5, a plurality of different stress times).

Claim 96. The method of claim 95, wherein said simulating the behavior (Chen: pg.245, right column, lines 13 and 14) is performed using a circuit simulator and includes incorporating the aging of the selected components (Rajgopal: column 8, lines 40-42) by updating the models of said circuit simulator.

Claim 97. The method of claim 1, wherein said simulating the behavior (Chen: pg.245, right column, lines 13 and 14) is performed using a circuit simulator and includes incorporating the aging of the selected components (Rajgopal: column 8, lines 40-42) by updating the models of said circuit simulator, and wherein said determining the degraded operation of the circuit at the supplied stress time values (Chen: pg. 246, figure 5, "stress times") by simulating the operation of the circuit with the each of the specified components (Rajgopal: column 8, lines 40-42) using the respective aging model (Chen: pg. 244 "Model Formation" equation 1 "Age parameter") information and respective component degradation parameter (Chen: pg. 243, left column 2nd paragraph, line 6) at the supplied stress time values.

Claim 98. The method of claim 1, wherein degradation parameter (Chen: pg. 243, left column 2nd paragraph, line 6) is a degradation level relative to circuit stress time (Chen: pg. 246, figure 5, plurality of stress times), the method further comprising: quantizing each of said relative degradation levels to one of a plurality of discrete values (Chen: pg. 246, equation 7 with line 1) (Chen: pg. 246, equation 7 with line 1) (Chen: pg. 246, equation 7 with line 1), and wherein said determining the degraded operation of the circuit includes determining the degraded operation of the circuit by simulating the operation of the circuit with the specified components (Rajgopal: column 8, lines 40-42) using their respective aging model (Chen: pg. 244 "Model Formation" equation 1 "Age parameter") information and respective quantized (age times as stated in spec. pg.6, lines 19-26: Chen pg. 246, figure 5 plurality of stress times or age times) relative

degradation level at the supplied circuit stress time (Chen: pg. 246, figure 5, plurality of stress times).

Claim 99. The method of claim 92, wherein the circuit includes a plurality of distinct sets of components, the process further comprising: supplying an independent performance criterion for each set of said plurality of distinct sets of components, and wherein said supplying aging model (Chen: pg. 244 "Model Formation" equation 1 "Age parameter") information includes supplying aging model (Chen: pg. 244 "Model Formation" equation 1 "Age parameter") information on selected components (Rajgopal: column 8, lines 40-42) from each of said sets of components, wherein each of the selected components' relative degradation parameter (Chen: pg. 243, left column 2nd paragraph, line 6) is determined using the respective performance criteria of the set to which the selected component belongs, and wherein said determining the degraded operation of the circuit includes determining the degraded operation of the circuit by simulating the operation of the circuit with each of the specified components (Rajgopal: column 8, lines 40-42)using the respective aging model (Chen: pg. 244 "Model Formation" equation 1 "Age parameter") information and respective relative component degradation parameter (Chen: pg. 243, left column 2nd paragraph, line 6) at the supplied circuit stress time (Chen: pg. 246, figure 5, plurality of stress times) values (Chen: pg. 246, figure 5, a plurality of different stress times).

Claim 100. The method of claim 92, wherein said supplying aging model (Chen: pg. 244 "Model Formation" equation 1 "Age parameter") information includes supplying aging model (Chen: pg. 244 "Model Formation" equation 1 "Age parameter") information on a first set of selected components (Rajgopal: column 8, lines 40-42) of the circuit and wherein said simulating the behavior (Chen: pg.245, right column, lines 13 and 14) of the fresh circuit (Chen: pg.243, left column, 2nd paragraph, lines 9-10) includes simulating the behavior (Chen: pg.245, right column, lines 13 and 14) of the fresh circuit (Chen: pg.243, left column, 2nd paragraph, lines 9-10)to determine for each of the first selected set of components (Rajgopal: column 8, lines 40-42) a component degradation parameter (Chen: pg. 243, left column 2nd paragraph, line 6) relative to circuit stress time (Chen: pg. 246, figure 5, plurality of stress times), the process further comprising: specifying the degradation level of a second set of selected components (Rajgopal: column 8, lines 40-42)of the circuit, wherein the elements of the first set and the second set of components (Rajgopal: column 8, lines 40-42)are distinct, and wherein said determining the degraded operation of the circuit includes determining the degraded operation of the circuit by simulating the operation of the circuit with each of the first set of specified components (Rajgopal: column 8, lines 40-42)using the respective aging model (Chen: pg. 244 "Model Formation" equation 1 "Age parameter") information and respective relative component degradation parameter (Chen: pg. 243, left column 2nd paragraph, line 6)at the supplied circuit stress time (Chen: pg. 246, figure 5, plurality of stress times) values (Chen: pg. 246, figure 5, a plurality of different stress times) and

with each of the second set of specified components (Rajgopal: column 8, lines 40-42) using the respective specified degradation level.

Claim 101. The method of claim 92, the process further comprising: revising the netlist (Rajgopal: column 5, line 63), wherein each of said selected components (Rajgopal: column 8, lines 40-42)is replaced by a non-aged ("Fresh" Chen, pg. 247, figure 11)version of the selected component and a plurality of independent current sources corresponding to different mechanisms connected between the terminals of the non-aged ("Fresh" Chen, pg. 247, figure 11)version, wherein the magnitude of the current relative to a circuit stress time (Chen: pg. 246, figure 5, plurality of stress times) in each of the current sources of a component is determined from the aging model (Chen: pg. 244 "Model Formation" equation 1 "Age parameter") information of the component and a distinct mechanism degradation parameter (Chen: pg. 243, left column 2nd paragraph, line 6) derived from the component degradation parameter; and wherein said determining the degraded operation of the circuit includes determining the degraded operation of the circuit by simulating the operation of the circuit with the revised netlist (Rajgopal: column 5, line 63 'revised netlist" user's discretion) at the supplied circuit stress time (Chen: pg. 246, figure 5, plurality of stress times) values (Chen: pg. 246, figure 5, a plurality of different stress times).

Claim 102. The method of claim 101, wherein said simulating the behavior (Chen: pg.245, right column, lines 13 and 14) is performed using a circuit simulator and

includes incorporating the aging of the selected components (Rajgopal: column 8, lines 40-42) by updating the models of said circuit simulator.

Claim 103. The method of claim 92, wherein said simulating the behavior (Chen: pg.245, right column, lines 13 and 14) is performed using a circuit simulator and includes incorporating the aging of the selected components (Rajgopal: column 8, lines 40-42) by updating the models of said circuit simulator, and wherein said determining the degraded operation of the circuit includes determining the degraded operation of the circuit at the supplied stress time values (Chen: pg. 246, figure 5, "stress times")by simulating the operation of the circuit with the each of the specified components (Rajgopal: column 8, lines 40-42) using the respective aging model (Chen: pg. 244 "Model Formation" equation 1 "Age parameter") information and respective relative component degradation parameter (Chen: pg. 243, left column 2nd paragraph, line 6) at the supplied stress time values.

Claim 104. The method of claim 92, wherein said degradation parameter (Chen: pg. 243, left column 2nd paragraph, line 6) is a degradation level relative to circuit stress time (Chen: pg. 246, figure 5, plurality of stress times), the process further comprising: quantizing each of said relative degradation levels to one of a plurality of discrete values (Chen: pg. 246, equation 7, with right column, line 1) and wherein said determining the degraded operation of the circuit includes determining the degraded

operation of the circuit by simulating the operation of the circuit with the specified components (Rajgopal: column 8, lines 40-42) using their respective aging model (Chen: pg. 244 "Model Formation" equation 1 "Age parameter") information and respective quantized (age times as stated in spec. pg.6, lines 19-26: Chen pg. 246, figure 5 plurality of stress times or age times) relative degradation level at the supplied circuit stress time (Chen: pg. 246, figure 5, plurality of stress times) value.

### *Section II: Response to Applicants' Arguments (Previous Office Action)*

#### *Claim Objection*

34. Objection to claim 91 is withdrawn.

#### *102(b)*

35. Applicants' arguments, see pages 15-26, filed 03/06/2006, with respect to the rejection of all claim active under 102(b) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground of rejection is made in view of Kadoch, Rajgopal, and Chen.

#### *Correspondence Information*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mr. Tom Stevens whose telephone number is 571-272-3715, Monday-Friday (8:00 am- 4:30 pm EST).

If attempts to reach the examiner by telephone are unsuccessful, please contact examiner's supervisor Mr. Paul Rodriguez 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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May 20, 2006

TS

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